16. Tus connection is not supporte irectly (xEN

4.2.4 Transmit channel

Signal name	

□ignal	Note
□□□_I	□eset
□LK_I	□loc□
AD□_I(:0)	-bit a □ res□ line
DA□_O(7:0)	8-bit receive ata
DA□_I(7:0)	8-bit tran□mit ata
WE_I	□ea /write
□□_□_I	□trobe
A□K_O	Ac□nowle ge
□Y□_I	□ycle
□AG0_O	□xDone interru□t
□AG1_O	□x□ea y interru□t

4 Des n descr pt n

4.1 Rec iv Cha nel

4.1.1 D si n not s

writing to this bit no further write operation to Tx FIFO buffer register is allowed till TxDone is set (all writes will be ignored).

- It is optional for the CPU to check the status bits of Tx status register.

4.6 Receive Frame

- The controller sets RxReady bit in Rx Status and control register (0x) and sets the RxReady interrupt line to indicate valid frame in internal buffer is available.
- It is recommended that the CPU read the Rx Status and control register (0x).
- The CPU should read the Frame length register (0x4) to check the size of the frame. The value of this regiter is valid only after the RxReady bit is set and remains valid till the first read from the Data buffer.
- The CPU should read Rx FIFO buffer register (0x) Frame length times to get all frame bytes. Performing extra reads (read from empty buffer) produces invalid data.
- If the CPU does not read all frame bytes as soon as possible the internal buffer will overflow and FIFOOverflow bit will be set and the current frame should be dropped. No further read operations should be attempted till RxReady bit is set again and RxReady interrupt is signaled indicating new available frame.
- The software can drop entire frame from the Receive FIFO buffer by writing 1 to drop bit in the status and control receive register (0x). This is suitable for dropping bad frames (for any reason) or frames with incorrect addresses.

4.7 Connection to TMS controller

The controller can get [illegible] get [illegible]

4. Block Diagram